AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 1 – 3, 14, 17, 20, 23, 25 – 29, 32 – 34, 45, 48, 49, 51, 53 – 57, 62 – 65, 69, 75, 85, 89, 91 – 94, 102 – 104, 106 – 110, 113, 114, 118, 119, 125, 126, 129 – 131, 135, 136, and 139, inclusive, and cancel claims 58, 81, 100, 117, and 122, as follows:

1 (Currently Amended). A system for adaptive configuration, the system comprising:

a memory adapted to store a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

a first plurality of fixed and differing computational elements;

a second plurality of fixed and differing computational elements; ~~and~~

an interconnection network coupled to the first and second pluralities of computational elements and to the memory, a first level of the interconnection network comprising ~~a plurality of switching elements and~~ a plurality of routing elements adapted to provide a selected operating mode of a plurality of operating modes by selectively routing data and the first and second subsets of configuration information to the corresponding first or second pluralities of computational elements, and a second level of the interconnection network comprising a plurality of switching elements adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to the first subset of configuration information, and ~~the interconnection network further adapted~~ to configure the second plurality of computational elements for a second, different functional mode of the plurality of functional modes, in response to the second subset of configuration information.

2 (Currently Amended). The system of claim 1, wherein the first set of configuration information provides a first system operating mode of the plurality of operating modes.

3 (Currently Amended). The system of claim 2, wherein the memory is further adapted to store a second set of configuration information, the second set of configuration information providing a second system operating mode of the plurality of operating modes.

4 (Previously Presented). The system of claim 3, wherein the first set of configuration information corresponds to a first system configuration capacity and the second set of configuration information corresponds to a second system configuration capacity.

5 (Original). The system of claim 1, wherein the first set of configuration information is selected from a plurality of sets of configuration information.

6 (Cancelled).

7 (Previously Presented). The system of claim 1, wherein the memory comprises a second plurality of computational elements configured for a memory functional mode.

8 (Previously Presented). The system of claim 1, wherein the memory comprises a configuration of the plurality of computational elements in response to the first set of configuration information.

9 (Previously Presented). The system of claim 1, wherein the first set of configuration information is transferred to the system from a machine-readable medium.

10 (Previously Presented). The system of claim 1, wherein the first set of configuration information is transmitted to the system through a wireless interface.

11 (Previously Presented). The system of claim 1, wherein the first set of configuration information is transmitted to the system through a wireline interface.

12 (Original). The system of claim 1, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

13 (Original). The system of claim 1, wherein the first set of configuration information is embodied as a stream of information data bits.

14 (Currently Amended). The system of claim 1, wherein the first and second pluralities of fixed and differing computational elements comprise ~~first fixed architecture and the second fixed architecture are selected from~~ a plurality of fixed circuit architectures, the plurality of fixed circuit architectures comprising a fixed architectures adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

15 (Previously Presented). The system of claim 1, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

16 (Original). The system of claim 1, wherein the first subset of configuration information and the second subset of configuration information are commingled with data to form a singular bit stream.

17 (Currently Amended). The system of claim 1, further comprising:

a controller coupled to the first and second pluralities ~~plurality~~ of computational elements and to the interconnection network, the controller adapted to direct and schedule the configuration of the first plurality of computational elements for

the first functional mode and the configuration of the second plurality of computational elements for the second functional mode.

18 (Previously Presented). The system of claim 17, wherein the controller is further adapted to time and schedule the configuration of the first and second pluralities of computational elements with corresponding data.

19 (Previously Presented). The system of claim 17, wherein the controller is further adapted to select the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

20 (Currently Amended). The system of claim 1, wherein when the second plurality of computational elements are configured for a controller functional ~~operating~~ mode of the plurality of functional modes, the second plurality of computational elements adapted to direct and schedule the configuration of the first plurality of computational elements for the first functional mode.

21 (Previously Presented). The system of claim 20, wherein the second plurality of computational elements is further adapted to time and schedule the configuration of the first plurality of computational elements with corresponding data.

22 (Previously Presented). The system of claim 20, wherein the second plurality of computational elements is further adapted to select the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

23 (Currently Amended). The system of claim 1, wherein the system is embodied within a mobile station having the a plurality of operating modes.

24 (Previously Presented). The system of claim 23, wherein the plurality of operating modes of the mobile station comprises at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

25 (Currently Amended). The system of claim 1, wherein the system is embodied within a server having the a plurality of operating modes.

26 (Currently Amended). The system of claim 1, wherein the system is embodied within an adjunct network entity having the a plurality of operating modes.

27 (Currently Amended). The system of claim 1, wherein the first plurality of computational elements are configured to generate a request for a second set of configuration information for a second system operating mode of the plurality of operating modes.

28 (Currently Amended). The system of claim 27, wherein the first plurality of computational elements are further configured to determine a system configuration ~~reconfiguration~~ capacity prior to utilizing the second set of configuration information to configure for the ~~reconfigure for a~~ second system operating mode.

29 (Currently Amended). The system of claim 28, wherein the system configuration ~~reconfiguration~~ capacity is determined in a plurality of predefined units of hardware.

30 (Previously Presented). The system of claim 1, wherein the system is embodied within an integrated circuit.

31 (Previously Presented). The system of claim 1, wherein the first plurality of computational elements are operating in the first functional mode while the second plurality of computational elements are being configured for the second functional mode.

32 (Currently Amended). A method for adaptive configuration of an integrated circuit, the integrated circuit having first and second pluralities of computational elements and an interconnection network, a first level of the interconnection network having routing elements and a second level of the interconnection network having switching elements, the method comprising:

receiving a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

using the routing elements, selectively routing data and the first subset of configuration information through the interconnection network to the first plurality of computational elements and selectively routing data and the second subset of configuration information through the interconnection network to the second plurality of computational elements to provide a selected operating mode of a plurality of operating modes;

in response to the first subset of configuration information, using the switching elements, configuring through the second level of the ~~an~~ interconnection network ~~a~~ the first plurality of computational elements for a first functional mode of a plurality of functional modes, the first plurality of computational elements having fixed and differing architectures;

in response to the second subset of configuration information, using the switching elements, configuring through the second level of the interconnection network the a second plurality of computational elements of the integrated circuit for a second, different functional mode of the plurality of functional modes. ~~modes; and~~

~~selectively routing, through the interconnection network, data and the first subset of configuration information to the first plurality of computational elements and data and the second subset of configuration information to the second plurality of heterogeneous computational elements.~~

33 (Currently Amended). The method of claim 32, wherein the first set of configuration information provides a first operating mode of the plurality of operating modes.

34 (Currently Amended). The method of claim 32, further comprising:

receiving a second set of configuration information, the second set of configuration information providing a second operating mode of the plurality of operating modes.

35 (Previously Presented). The method of claim 34, wherein the first set of configuration information corresponds to a first configuration capacity and the second set of configuration information corresponds to a second configuration capacity.

36 (Original). The method of claim 32, further comprising:

selecting the first set of configuration information from a plurality of sets of configuration information.

37 (Original). The method of claim 32, further comprising:

storing the first set of configuration information in a memory.

38 (Previously Presented). The method of claim 32, further comprising:

storing the first set of configuration information in a second plurality of heterogeneous computational elements configured for a memory functional mode.

39 (Previously Presented). The method of claim 32, further comprising:

storing the first set of configuration information as a configuration of the plurality of heterogeneous computational elements.

40 (Original). The method of claim 32, further comprising:

storing the first set of configuration information in a machine-readable medium.

41 (Previously Presented). The method of claim 32, wherein the first set of configuration information is received through a wireless interface.

42 (Original). The method of claim 32, wherein the first set of configuration information is received through a wireline interface.

43 (Original). The method of claim 32, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

44 (Original). The method of claim 32, wherein the first set of configuration information is embodied as a stream of information data bits.

45 (Currently Amended). The method of claim 32, wherein the first and second pluralities of fixed and differing computational elements comprise ~~first fixed architecture and the second fixed architecture are selected from~~ a plurality of fixed circuit architectures, the plurality of fixed circuit architectures comprising circuitry adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

46 (Previously Presented). The method of claim 32, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

47 (Original). The method of claim 32, wherein the first subset of configuration information and the second subset of configuration information are commingled with data to form a singular bit stream.

48 (Currently Amended). The method of claim 32, further comprising:

directing and scheduling the configuration of the first plurality of fixed and differing ~~heterogeneous~~ computational elements for the first functional mode and the

~~reconfiguration of the plurality of heterogeneous~~ configuration of the second plurality of fixed and differing computational elements for the second functional mode.

49 (Currently Amended). The method of claim 32, further comprising:

timing and scheduling the configurations of the first and second pluralities of fixed and differing ~~configuration and reconfiguration of the plurality of heterogeneous~~ computational elements with corresponding data.

50 (Original). The method of claim 32, further comprising:

selecting the first subset of configuration information and the second subset of configuration information from a singular bit stream containing data commingled with the first set of configuration information.

51 (Currently Amended). The method of claim 32, wherein the method is operable within a mobile station having the a plurality of operating modes.

52 (Previously Presented). The method of claim 51, wherein the plurality of operating modes of the mobile station comprises at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

53 (Currently Amended). The method of claim 32, wherein the method is operable within a server having the a plurality of operating modes.

54 (Currently Amended). The method of claim 32, wherein the method is operable within an adjunct network entity having the a plurality of operating modes.

55 (Currently Amended). The method of claim 32, further comprising:

configuring the first plurality of fixed and differing computational elements ~~plurality of heterogeneous computational elements~~ to generate a request for a

second set of configuration information, the second set of configuration information providing a second operating mode of the plurality of operating modes.

56 (Currently Amended). The method of claim 55, further comprising:

determining configuration ~~reconfiguration~~ capacity prior to utilizing the second set of configuration information to configure ~~reconfigure~~ the second plurality of fixed and differing ~~heterogeneous~~ computational elements for the ~~a~~ second operating mode.

57 (Currently Amended). The method of claim 56, wherein configuration ~~reconfiguration~~ capacity is determined in a plurality of predefined units of hardware.

58 (Cancelled).

59 (Original). The method of claim 32, further comprising:

authorizing the reception of the first set of configuration information.

60 (Original). The method of claim 32, further comprising:

requesting authorization to receive the first set of configuration information.

61 (Original). The method of claim 32, further comprising:

decrypting the first set of configuration information.

62 (Currently Amended). The method of claim 32, further comprising:

operating ~~a~~ the first ~~portion of the~~ plurality of fixed and differing ~~heterogeneous~~ computational elements in the first functional mode while configuring the ~~a~~ second ~~portion of the~~ plurality of fixed and differing ~~heterogeneous~~ computational elements for the second functional mode.

63 (Currently Amended). A method for adaptive configuration of an integrated circuit, the integrated circuit having an interconnection network and first and second pluralities of fixed and differing computational elements, a first level of the interconnection network having routing elements and a second level of the interconnection network having switching elements, the method comprising:

transmitting a first set of configuration information, the first set of configuration information comprising a first subset of configuration information and a second subset of configuration information;

wherein when the first set of configuration information is received: ~~received,~~

using the routing elements, selectively routing data and the first subset of configuration information through the interconnection network to the first plurality of computational elements and selectively routing data and the second subset of configuration information through the interconnection network to the second plurality of computational elements to provide a selected operating mode of a plurality of operating modes; and

using the switching elements, configuring through the second level of the ~~an~~ interconnection network the ~~a~~ first plurality of fixed and differing computational elements for a first functional mode of a plurality of functional modes in response to the first subset of configuration information, and the ~~a~~ second plurality of fixed and differing computational elements for a second, different functional mode of the plurality of functional modes in response to the second subset of configuration information. ~~information; and~~

~~selectively routing, through the interconnection network, data and the first subset of configuration information to the first plurality of computational elements and data and the second subset of configuration information to the second plurality of heterogeneous computational elements.~~

64 (Currently Amended). The method of claim 63, wherein the first set of configuration information, when received, provides a first operating mode of the plurality of operating modes.

65 (Currently Amended). The method of claim 64, further comprising:

transmitting a second set of configuration information, the second set of configuration information, when received, providing a second operating mode of the plurality of operating modes.

66 (Previously Presented). The method of claim 65, wherein the first set of configuration information corresponds to a first configuration capacity and the second set of configuration information corresponds to a second configuration capacity.

67 (Original). The method of claim 63, further comprising:

selecting the first set of configuration information from a plurality of sets of configuration information.

68 (Currently Amended). The method of claim 63, further comprising:

accessing the first set of configuration information in the ~~a~~ memory.

69 (Currently Amended). The method of claim 63, further comprising:

accessing the first set of configuration information in a third ~~second~~ plurality of ~~heterogeneous~~ computational elements configured for a memory functional mode.

70 (Original). The method of claim 63, further comprising:

accessing the first set of configuration information in a machine-readable medium.

71 (Previously Presented). The method of claim 63, wherein the first set of configuration information is transmitted through a wireline interface.

72 (Original). The method of claim 63, wherein the first set of configuration information is transmitted through a wireline interface.

73 (Original). The method of claim 63, wherein the first set of configuration information is embodied as a plurality of discrete information data packets.

74 (Original). The method of claim 63, wherein the first set of configuration information is embodied as a stream of information data bits.

75 (Currently Amended). The method of claim 63, wherein the first and second pluralities of fixed and differing computational elements comprise ~~first fixed architecture and the second fixed architecture are selected from~~ a plurality of fixed architectures, the plurality of fixed architectures comprising circuitry adapted to perform at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

76 (Previously Presented). The method of claim 63, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

77 (Original). The method of claim 63, wherein the transmission step further comprises commingling data with the first subset of configuration information and the second subset of configuration information to form a singular bit stream.

78 (Original). The method of claim 63, wherein the method is operable within a wireless transmitter.

79 (Original). The method of claim 63, wherein the method is operable within a server.

80 (Original). The method of claim 63, wherein the method is operable within an adjunct network entity.

81 (Cancelled).

82 (Original). The method of claim 63, wherein the method is operable within a local area network.

83 (Original). The method of claim 63, wherein the method is operable within a wide area network.

84 (Original). The method of claim 63, wherein the method is operable within a wireline transmitter.

85 (Currently Amended). The method of claim 63, further comprising:

receiving a request for transmission of a second set of configuration information, the second set of configuration information providing a second operating mode of the plurality of operating modes.

86 (Original). The method of claim 63, further comprising:

authorizing the transmission of the first set of configuration information.

87 (Original). The method of claim 63, further comprising:

requesting an authorization to transmit the first set of configuration information.

88 (Original). The method of claim 63, further comprising:

encrypting the first set of configuration information.

89 (Currently Amended). An integrated circuit, comprising:

a memory adapted to store configuration information, the configuration information comprising first configuration information and second configuration information;

a plurality of configurable matrices, at least two configurable matrices of the plurality of configurable matrices each comprising a first interconnection network and ~~plurality~~ different pluralities of fixed and differing computational elements, ~~the~~ each corresponding plurality ~~plurality~~ of fixed and differing computational elements coupled to the corresponding first ~~an~~ interconnect network and configurable for a corresponding functional mode through configuration of a plurality of input and output connections by the corresponding first interconnection network in response to the configuration information; and

a second, matrix interconnection network coupled to the plurality of configurable matrices, the matrix interconnection network adapted to configure the plurality of configurable matrices for a selected operating mode of a plurality of operating modes by selectively transferring ~~transfer~~ data and configuration information to the plurality of configurable matrices.

90 (Previously Presented). The integrated circuit of claim 89, further comprising:

a controller coupled to the plurality of reconfigurable matrices, the controller adapted to direct a transfer of the configuration information from the memory to the reconfigurable matrices.

91 (Currently Amended). An integrated circuit, comprising:

a memory adapted to store a set of configuration information, the set of configuration information comprising a first ~~subset of~~ configuration information and a second ~~subset of~~ configuration information;

first and second pluralities of heterogeneous computational elements;

a plurality of ~~an~~ interconnection networks ~~network~~ coupled to the first and second pluralities of heterogeneous computational elements, a first ~~the~~ interconnection network of the plurality of interconnection networks comprising a plurality of routing elements capable of differentially routing data and configuration information to the first and second pluralities of heterogeneous computational elements, a second interconnection network of the plurality of interconnection networks comprising a first plurality ~~and a first and second pluralities of switching elements, the first plurality~~ of switching elements capable of configuring the first plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first ~~subset of~~ configuration information, and a third interconnection network of the plurality of interconnection networks comprising a ~~the~~ second plurality of switching elements capable of configuring the second plurality of heterogeneous computational elements for a second, different functional mode of the plurality of functional modes in response to the second configuration information. ~~subset of configuration information, the routing elements capable of differentially routing data and configuration information to the first and second pluralities of heterogeneous computational elements~~.

92 (Currently Amended). The integrated circuit of claim 91, wherein the second interconnection network is coupled to the first plurality of heterogeneous computational elements and wherein the third interconnection network is coupled to the second plurality of heterogeneous computational elements. ~~first subset of the plurality of heterogeneous computational elements are distributed among the plurality of heterogeneous computational elements~~.

93 (Currently Amended). An adaptive integrated circuit, comprising:

a memory adapted to store configuration information;

an input and output interface;

a plurality of computational elements having fixed and differing circuit architectures;

a first ~~an~~ interconnection network coupled to the plurality of computational elements, the first interconnection network comprising a plurality of ~~routing elements and a plurality of~~ switching elements~~, the interconnection network~~ capable of configuring the plurality of computational elements for a plurality of functional modes in response to the configuration information by selectively ~~routing data to the plurality of computational elements and selectively~~ switching input and output connections between selected computational elements of the plurality of computational elements; and ~~elements.~~

a second interconnection network coupled to the interface, to the plurality of computational elements and to the first interconnection network, the second interconnection network comprising a plurality of routing elements capable of providing a selected functional mode of the plurality of functional modes in response to the configuration information by selectively routing data packets to selected computational elements of the plurality of computational elements and selectively routing configuration information packets to the first interconnection network.

94 (Currently Amended). An integrated circuit, comprising:

a first plurality of fixed and differing computational elements; and

an interconnection network coupled to the first plurality of computational elements, the interconnection network comprising a plurality of routing elements, the interconnection network adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to first configuration information by selectively routing addressed data packets through the routing elements and to selected computational elements of the first plurality of computational elements.

95 (Previously Presented). The integrated circuit of claim 94, wherein the first configuration information provides an operating mode.

96 (Previously Presented). The integrated circuit of claim 94, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

97 (Previously Presented). The integrated circuit of claim 94, wherein the first configuration information is stored in at least one computational element, of the first plurality of computational elements, configured for a memory functional mode.

98 (Previously Presented). The integrated circuit of claim 94, wherein the first configuration information is stored as a configuration of the first plurality of computational elements.

99 (Previously Presented). The integrated circuit of claim 94, wherein the first plurality of computational elements are selected from a plurality of fixed circuitry architectures, the plurality of fixed circuitry architectures comprising circuitry adapted to perform at least two of the following functions: memory, addition, multiplication,

complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

100 (Cancelled).

101 (Previously Presented). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network, the second plurality of computational elements comprising at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

102 (Currently Amended). The integrated circuit of claim 101, wherein the interconnection network is further adapted to independently configure the first plurality of computational elements in response to the first configuration information and configure the second plurality of computational elements in response to second configuration information by selectively routing addressed data packets through the routing elements to the addressed first plurality of computational elements or to the addressed second plurality of computational elements.

103 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively routing data packets and control information packets to the first plurality of computational elements and the second plurality of computational elements.

104 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, and wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data between computational elements of ~~to~~ the first plurality of computational elements and the second plurality of computational elements.

105 (Previously Presented). The integrated circuit of claim 104, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

106 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, and wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching ~~or~~ and routing data between computational elements of ~~to~~ the first plurality of computational elements and the second plurality of computational elements.

107 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes

by selectively routing data between computational elements of ~~to~~ the first plurality of computational elements and the second plurality of computational elements.

108 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively switching data between computational elements of ~~to~~ the first plurality of computational elements and the second plurality of computational elements.

109 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the interconnection network is further adapted to configure the second plurality of computational elements in response to second configuration information; and

wherein the interconnection network is further adapted to selectively route data and the first ~~subset of~~ configuration information to the first plurality of computational elements and route data and the second ~~subset of~~ configuration information to the second plurality of computational elements.

110 (Currently Amended). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the plurality of routing elements are adapted for self-routing of the addressed data packets to the first and second pluralities of computational elements.

111 (Previously Presented). The integrated circuit of claim 94, further comprising:

a second plurality of fixed and differing computational elements coupled to the interconnection network;

wherein the plurality of routing elements are adapted for self-routing of first configuration information to the first plurality of computational elements and self-routing of second configuration information to the second plurality of computational elements.

112 (Previously Presented). The integrated circuit of claim 94, further comprising:

a memory coupled to the interconnection network, the memory adapted to store the first configuration information.

113 (Currently Amended). The integrated circuit of claim 94, wherein the interconnection network further comprises a plurality of switching elements and a data interface circuit, and wherein the interconnection network is further adapted to configure the first plurality of computational elements by selectively routing the data packets through the data interface circuit for transfer to the first plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

114 (Currently Amended). The integrated circuit of claim 94, further comprising:

a data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

wherein the interconnection network further comprises a plurality of switching elements, wherein the plurality of routing elements of the interconnection network are adapted to selectively route the data packets to the data interface circuit for transfer to the first plurality of computational elements, and wherein the plurality of switching elements of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output

connections between the computational elements comprising the first plurality of computational elements.

115 (Previously Presented). The system of claim 1, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements.

116 (Previously Presented). The system of claim 1, wherein the interconnection network is further adapted to independently configure the first plurality of computational elements and the second plurality of computational elements.

117 (Cancelled).

118 (Currently Amended). The system of claim 1, wherein the first level of the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

119 (Currently Amended). The system of claim 1, wherein the second plurality of computational elements further comprises at least one computational element which is different than the computational elements comprising the first plurality of computational elements, and wherein the first level of the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

120 (Previously Presented). The system of claim 1, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third

functional mode of the plurality of functional modes by selectively routing data to the first plurality of computational elements and the second plurality of computational elements.

121 (Previously Presented). The system of claim 1, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

122 (Cancelled).

123 (Previously Presented). The system of claim 1, wherein the plurality of routing elements are adapted for self-routing of data packets to the first and second pluralities of computational elements.

124 (Previously Presented). The system of claim 1, wherein the plurality of routing elements are adapted for self-routing of the first subset of configuration information to the first plurality of computational elements and self-routing of the second subset of configuration information to the second plurality of computational elements.

125 (Currently Amended). The system of claim 1, wherein the interconnection network further comprises a first data interface circuit coupled to the first plurality of computational elements and a second data interface circuit coupled to the second plurality of computational elements, wherein the first level of the interconnection network is further adapted to configure the first plurality of computational elements by selectively routing data through the first data interface circuit for transfer to the first plurality of computational elements, wherein the second level of the interconnection network is further adapted to ~~and~~ selectively switch ~~switching~~ data input and output connections between the computational elements comprising the first plurality of computational

elements, ~~and~~ wherein the first level of the interconnection network is further adapted to configure the second plurality of computational elements by selectively routing data through the second data interface circuit for transfer to the second plurality of computational elements, and wherein the second level of the interconnection network is further adapted to ~~and~~ selectively switch ~~switching~~ data input and output connections between the computational elements comprising the second plurality of computational elements.

126 (Currently Amended). The system of claim 1, further comprising:

a first data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

a second data interface circuit coupled to the second plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements of the first level of the interconnection network are adapted to route data selectively to the first data interface circuit for transfer to the first plurality of computational elements and to the second data interface circuit for transfer to the second plurality of computational elements, wherein the plurality of switching elements of the second level of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements, and wherein the plurality of switching elements of the second level of the interconnection network are adapted to configure the second plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the second plurality of computational elements.

127 (Previously Presented). The system of claim 1, wherein the plurality of switching elements comprise a plurality of multiplexers.

128 (Previously Presented). The system of claim 1, wherein the plurality of switching elements comprise a plurality of demultiplexers.

129 (Currently Amended). An integrated circuit, comprising:

a first plurality of fixed and differing computational elements forming a first configurable architecture;

an interconnection network coupled to the first plurality of computational elements, ~~the~~ a first level of the interconnection network adapted to selectively transfer data, in response to first configuration information, between selected computational elements of the first plurality of computational elements, and a second level of the interconnection network adapted to transfer data ~~and first configuration information~~ selectively to a selected computational element of the first plurality of computational elements and to transfer the first configuration information selectively to the first level of the interconnection network.

130 (Currently Amended). The integrated circuit of claim 129, wherein the second level of the interconnection network comprises a plurality of routing elements and wherein the first level of the interconnection network comprises a plurality of switching elements.

131 (Currently Amended). The integrated circuit of claim 130, further comprising:

a second plurality of fixed and differing computational elements forming a second, different configurable architecture; and

a corresponding first level of the interconnection network coupled to the second plurality of computational elements, the corresponding first level of the interconnection network adapted to selectively transfer data, in response to second configuration information, between selected computational elements of the second plurality of computational elements;

wherein the second level of the interconnection network is further adapted to transfer data ~~and second configuration information~~ selectively to the second ~~first~~ plurality of computational elements and to transfer the second configuration information selectively to the corresponding first level of the interconnection network.

132 (Previously Presented). The integrated circuit of claim 131, wherein the interconnection network is further adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information and to independently configure the second plurality of computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information.

133 (Previously Presented). The integrated circuit of claim 132, wherein the interconnection network is further adapted to configure the first plurality of computational elements and the second plurality of computational elements by selectively routing or selectively switching data to the first plurality of computational elements and the second plurality of computational elements.

134 (Previously Presented). The integrated circuit of claim 132, wherein the interconnection network is further adapted to additionally configure both the first plurality of computational elements and the second plurality of computational elements for a third functional mode of the plurality of functional modes by selectively routing or switching data to the first plurality of computational elements and the second plurality of computational elements.

135 (Currently Amended). The integrated circuit of claim 130, wherein the plurality of routing elements of the second level of the interconnection network are adapted for self-routing of data packets to the first plurality of computational elements.

136 (Currently Amended). The integrated circuit of claim 130, wherein the plurality of routing elements of the second level of the interconnection network are adapted for self-routing of first configuration information to the first level of the interconnection network. ~~plurality of computational elements.~~

137 (Previously Presented). The integrated circuit of claim 130, wherein the interconnection network further comprises a data interface circuit, and wherein the

interconnection network is further adapted to configure the first plurality of computational elements by selectively routing data through the data interface circuit for transfer to the first plurality of computational elements and selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

138 (Previously Presented). The integrated circuit of claim 130, further comprising:

a data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements of the interconnection network are adapted to selectively route data to the data interface circuit for transfer to the first plurality of computational elements, and wherein the plurality of switching elements of the interconnection network are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements.

139 (Currently Amended). An integrated circuit, comprising:

a first plurality of fixed and differing computational elements forming a first configurable ~~reconfigurable~~ circuit;

a second plurality of fixed and differing computational elements forming a second, different configurable circuit; and

an interconnection network coupled to the first and second pluralities of computational elements, the interconnection network comprising a plurality of routing elements and a plurality of switching elements, the interconnection network adapted to configure the first plurality of computational elements for a first functional mode of a plurality of functional modes in response to first configuration information and to independently configure the second plurality of computational elements in response to second configuration information by selectively routing data through the routing elements ~~or~~ and selectively switching data through the switching elements to the first plurality of computational elements and the second plurality of computational elements.

140 (Previously Presented). The integrated circuit of claim 139, wherein the interconnection network is further adapted to selectively route data and the first configuration information to the first plurality of computational elements and route data and the second configuration information to the second plurality of computational elements.

141 (Previously Presented). The integrated circuit of claim 139, wherein the plurality of routing elements are adapted for self-routing of data packets to the first and second pluralities of computational elements.

142 (Previously Presented). The integrated circuit of claim 139, wherein the plurality of routing elements are adapted for self-routing of first configuration information to the first plurality of computational elements and self-routing of second configuration information to the second plurality of computational elements.

143 (Previously Presented). The integrated circuit of claim 139, further comprising:

a first data interface circuit coupled to the first plurality of computational elements and to the interconnection network;

a second data interface circuit coupled to the second plurality of computational elements and to the interconnection network;

wherein the plurality of routing elements are adapted to selectively route data to the first data interface circuit for transfer to the first plurality of computational elements and to selectively route data to the second data interface circuit for transfer to the second plurality of computational elements, and wherein the plurality of switching elements are adapted to configure the first plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the first plurality of computational elements and to configure the second plurality of computational elements by selectively switching data input and output connections between the computational elements comprising the second plurality of computational elements.